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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/607,286 | 06/25/2003 | Philip S. Ng | ATM-255 | 4958 |

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| EXAMINER | |
|---|---|
| TON, MY TRANG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/607,286 | NG ET AL. | |
| | Examiner | Art Unit | |
| | My-Trang N. Ton | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "at least one transistor switch having a gate connected to said data output of said flip-flop" recited in claim 1, "the gates of a plurality of transistor switches being connected to the data outputs of a plurality of flip-flops" recited in claims 2 and 14, "a set of transistor switches each having a gate connected to said data output of each said flip-flop" recited in claim 6, "a set of flip-flops connected to the gates of said switching transistors" recited in claim 10, "outputs of said flip-flops being connected to controlling terminals of a plurality of switches" recited in claim 15 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The description of the present invention in claim 1 is indefinite since it fails to establish the proper structural and/or functional relationship between the recited circuit elements. Applicant is required to particularly point out how the limitations of claim 1

read on the circuit arrangement of the drawing. For example, claim 1 calls for "at least one transistor switch having a gate connected to said data output of said flip-flop" which is not seen in the preferred embodiment of the invention. Clearly, as shown in Fig. 3, at least one transistor switch 60 having a gate connected to Default = "0" or Vcc, or at least one transistor switch 62 having a gate connected to Default = "1" or Ground. The common output of 60 and 62 is connected to an output of flip-flops 30, 32... Moreover, the limitation "a state of said switcher is established by a state of said flip-flop" is misdescriptive of the present invention. How does this occur?

Claim 2 recites the limitation "plurality of transistor switches" in line 2. There is insufficient antecedent basis for this limitation in the claim. Moreover, claim 2 is similarly rejected as claim 1 regarding "the gates of a plurality of transistor switches being connected to the data outputs of a plurality of flip-flops".

Claims 6, 10, 14, 15 contain the same problems as the above claims 1-2, and are similarly rejected.

Claims 3-5, 7-9, 11-13, 16 are rendered indefinite by the deficiencies of claims 1, 6, 10, 15.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14 are, insofar as understood, rejected under 35 U.S.C. 102(b) as being anticipated by Maekawa (U.S Patent No. 5,708,455).

Maekawa discloses in Figs 1-5 an active matrix display device including:

at least one flip-flop (2, SHIFT REGISTER) having a data input (IN), a data output (OUT), and a control input (CK, CKX),

at least one transistor switch (3), due to the indefinite, the limitation "at least one transistor switch having a gate connected to said data output of said flip-flop" does not given sufficient weight to read over the reference as recited in claim 1.

Regarding claim 2, the limitation "the gates of a plurality of transistor switches being connected to the data outputs of a plurality of flip-flops" does not give sufficient weight to read over the reference as recited in claim 1. Elements R, L reads on "a plurality of transistor switches"; and element 2 SHIFT REGISTER reads on "a shift register".

Regarding claim 3, the data output (OUT) of said flip-flop (2) further connects to a default value generating means (RT and RTX).

Element RT reads on a first default signal line, element RTX reads on a second default signal line, RTX carries a complementary signal to RT, the limitation "buffering means" is inherent seen in RTX (which is an inversion of RT) as recited in claim 4.

The limitation "buffering means being a MOS transistor" is inherent seen in RTX (which is an inversion of RT, each inverter contains MOS transistor) as recited in claim 5.

Claims 6-14 are similarly rejected a claims 1-5.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 1, 2004

MY-TRANG NU TON
PRIMARY EXAMINER